METHOD TO PREDICT DIELECTRIC FILM PROPERTIES USING CHEMICAL BONDING MEASUREMENTS AS INPUT TO COMPUTER MODELING

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The invention relates to the fabrication of integrated circuit devices, and more particularly, to a method for determining dielectric film properties. The method of the invention uses computer modeling of dielectric film properties whereby chemical bonding measurements are the input data that is provided to the computer model.

(2) Description of the Prior Art

Dielectric materials are arguably one of the most frequently applied materials in the creation of semiconductor devices. A wide range of materials can be used as a dielectric material, such materials can for instance contain silicon dioxide ("oxide", doped or undoped) or silicon nitride ("nitride"), silicon oxynitride, fluoropolymer, parylene, polyimide, tetra-ethyl-ortho-silicate (TEOS) based oxides, boro-phosphate-silicate-glass (BPSG), phospho-silicate-glass (PSG), boro-silicate-glass (BSG), oxide-nitride-oxide (ONO), a low dielectric constant material, such as hydrogen silsesquioxane and HDP-FSG (high-density-plasma

fluorine-doped silicate glass. The most commonly used and therefore the preferred dielectrics are silicon dioxide (doped or undoped), silicon oxynitride, parylene or polyimide, spin-on-glass, plasma oxide or LPCVD oxide. The preferred dielectric material to be used for the invention is SiO_2.

Typical conditions for the deposition of a layer of dielectric uses, for instance, PECVD procedures at a temperature of between about 350 and 450 degrees C. to a thickness between about 5000 and 10,000 Angstrom using TEOS as a source. The preferred etching conditions for the TEOS etch are using CF_4 or CHF_3 as the etchant gas at a flow rate of about 15 sccm, gas pressure about 800 mTorr, rf power density about 400 Watts, with no magnetic field applied, ambient wafer temperature with a time of the etch of about 10 seconds.

One of the more interesting dielectric materials that has received increased attention and application is conventional polyimides, which have a number of attractive characteristics for their application in a semiconductor device structure such as the ability to fill openings of high aspect ratio, a relatively low dielectric constant (about 3.2), a simple process required for the depositing of a layer of polyimide, the reduction of sharp features or steps in the underlying

layer, high temperature tolerance of cured polyimide. Photosensitive polyimides have these same characteristics but can, in addition, be patterned like a photoresist mask and can, after patterning and etching, remain on the surface on which it has been deposited to serve as a passivation layer. The process of depositing and patterning polyimide is relatively simple and is well understood in the art. Polyimide is typically spun on in the form of a liquid (polyamic-acid precursor). After spin-on, the polyimide may be cured whereby the spun-on polyimide becomes a solid polyimide film. Etching of the cured film often uses oxygen or fluorine based plasma. Polyimide is typically applied over the entire substrate followed by a baking step to cure and evaporate the solvents in the polyimide. Curing of the polyimide provides extra protection to the device circuitry. This step is typically a high temperature cure, at 350 to 400 degrees C., in a N_2 gas ambient for a time period between about 1.5 and 2.5 hours. Polyimide provides extra protection to the surface of the silicon chip against scratching, cracking and other types of mechanical damage. Most often, mechanical damage occurs during assembly, packaging or any subsequent handling of the die. As a passivation layer, polyimide also guards against thin film cracking which frequently results from the packaging of very large dies into plastic packages. A passivation layer can contain silicon oxide/silicon nitride (SiO_2/Si_3N_4) deposited

by CVD, a passivation layer can however also be a photosensitive polyimide or can comprise titanium nitride. Another material often used for passivation layer is phosphorous doped silicon dioxide that is typically deposited over a final layer of aluminum interconnect using a Low Temperature CVD process.

Dielectric materials find numerous applications in the formation of semiconductor devices. For instance, spacers that are formed on the sidewalls of gate electrodes can be made using silicon-nitride or silicon-oxide, BSG, PSG, polysilicon, other materials preferably of a dielectric nature, CVD oxide formed from a TEOS source. Often used are amorphous materials that inhibit the deposition of epitaxial silicon thereupon. A silicon oxide spacer can be formed via anisotropic RIE of said silicon oxide layer, using CHF_3 or CF_4-O_2-He as an etchant. A silicon nitride spacer can be formed via anisotropic RIE of said silicon nitride layer, using CHF_3 or SF_6-O_2 as an etchant.

Dielectric materials are frequently used for the creation of conductive interconnect lines, via or contact openings. In the formation of semiconductor integrated circuits, it is common practice to form interconnect metal line structures on a number of different levels within the structure and interconnecting

the various levels of wiring with contact or via openings. The first or lowest level of interconnect wires is typically formed in a layer of dielectric as a first step in the process after which a second or overlying level of interconnect wires is created in an overlying layer of dielectric over the first level. The first level of interconnect wires is typically in contact with active regions in a semiconductor substrate but is not limited to such contact. The first level of interconnect can for instance also be in contact with a conductor that leads to other devices that form part of a larger, multi-chip structure. The two levels of metal wires are connected by openings between the two layers that are created in the layers of surrounding dielectric and that are filled with metal where the openings between the two layers are lines up with and match contact points in one or both of the levels of metal lines.

Previously used techniques to form multi-levels of wiring apply the technique of first forming the interconnect level metal in a first plane followed by forming the overlying level of interconnect wire in a second plane. This structure typically starts with the surface of a semiconductor substrate into which active devices have been created. The surface into which the pattern of interconnect lines of the first plane is formed may also be an insulation layer deposited over the surface of the substrate or a layer of oxide may first have been formed on the surface of the substrate. After the layer, into which

the pattern of interconnecting wires has to be created, has been defined, the interconnecting pattern itself needs to be defined. This is done using conventional photolithographic techniques whereby the openings are made (in the layer) above the points that need to be contacted in the substrate. The openings, once created, may by lined with layers of material to enhance metal adhesion (to the sidewalls of the opening), the glue layer, or to prevent diffusion of materials into and from the substrate in subsequent processing steps, the barrier layer. For the barrier layer, a variety of materials can be used such as Ti/Tin:W (titanium/titanium nitride:tungsten), titanium-tungsten/titanium or titanium-tungsten nitride/titanium or titanium nitride or titamium nitride/titanium, silicon nitride (Si_3N_4), tungsten, tantalum, niobium, molybdenum. The final phase in creating the first level of interconnect lines is to fill the created openings with metal, typically aluminum, tungsten or copper, dependent on the particular application and requirements and restrictions imposed by such parameters as line width, aspect ratio of the opening, required planarity of the surface of the deposited metal and others.

This process of line formation in overlying layers on metal can be repeated in essentially the same manner as just highlighted for the first layer of interconnecting wires. This process of forming sequential layers of interconnecting levels of wire is in many instances prone to problems and limitations.

Copper has in recent times found more application in the use of metal wires due to its low resistivity, high electromigration resistance and stress voiding resistance. Copper however exhibits the disadvantage of high diffusivity in common insulating materials such as silicon dioxide and oxygen-containing polymers. This leads to, for instance, the diffusion of copper into polyimide during high temperature processing of the polyimide resulting in severe erosion of the copper and the polyimide due to the copper combining with oxygen in the polyimide. The erosion may result in loss of adhesion, delamination, voids, and ultimately a catastrophic failure of the component. The copper that is used in an interconnect may diffuse into the silicon dioxide layer causing the dielectric strength to become conductive and also decreasing the dielectric strength of the silicon dioxide layer. A copper diffusion barrier is therefore often required; silicon nitride is often applied as a diffusion barrier to copper. Silicon nitride however has a dielectric constant that is high compared to silicon dioxide thereby limiting the use of silicon nitride in encapsulating copper interconnect lines. To further enhance the adhesion of a copper interconnect line to the surrounding layer of dielectric or insulation, a seed layer is deposited over the barrier layer. A seed layer can be deposited using a sputter chamber or an Ion Metal Plasma (IMP) chamber at a temperature of between about 0

and 300 degrees C. and a pressure of between about 1 and 100 mTorr, using copper or a copper alloy as the source at a flow rate of between about 10 and 400 sccm and using argon as an ambient gas. The minimum thickness of a seed layer is about 50 Angstrom, this thickness is required achieve a reliable gap fill.

Scaling devices to smaller dimensions can lead to a multitude of undesirable effects. One of these effects is the increase in the capacitive coupling between conductors in the circuit. Therefore, it becomes impractical to reduce the RC time constant and cross talk between metal lines within today's multi-level metallization system.

The capacitance between conductors is highly dependent on the insulator or dielectric used to separate the lines. Conventional semiconductor fabrication commonly employs silicon dioxide as a dielectric that has a dielectric constant of about 3.9. The lowest possible, or ideal, dielectric constant is 1.0, which is the dielectric constant of a vacuum.

For a given interconnect layout, both power consumption and crosstalk decrease, and performance increases, as the dielectric constant of the insulator decreases. It has been found that using the same dielectric, scaling down from 0.50 um. to 0.25 um. will

result in a 30% increase in power consumption. This power consumption can be decreased by more than 50% if SiO_2 is replaced by oxide. This change is important for high frequency operation because power consumption increases proportionally with frequency.

Additionally, the crosstalk increases more than 50% when scaling down from 0.50 um. to 0.25 um. primarily due to the increase in line-to-line capacitance. The increase in the ration crosstalk/Vcc degrades the noise margin and circuit performance. Replacing SiO_2 with air will significantly reduce crosstalk because of the small dielectric constant of air, which is generally less than 1.001.

In the field of high density interconnect technology, many integrated circuit chips are physically and electrically connected to a single substrate commonly referred to as a multi-chip module (MCM). To achieve a high wiring and packing density, it is necessary to fabricate a multilayer structure on the substrate to connect integrated circuits to one another. Typically, metal power and ground planes in the substrate are separated by layers of a dielectric such as a polyimide. Embedded in other dielectric layers are metal conductor lines within the range of about 8 to 25p wide) with vias (holes) providing

electrical connections between signal lines or to the metal power and ground planes. Adjacent layers are ordinarily formed so that the primary signal propagation directions are orthogonal to each other. Since the conductor features are typically narrow in width and thick in a vertical direction (in the range of 5 to 10 microns thick) and must be patterned with microlithography, it is important to produce patterned layers that are substantially flat and smooth (i.e. planar) to serve as the base for the next layer.

From the above highlighted applications of dielectric materials in the formation of semiconductor devices, the following performance characteristics that apply to dielectric materials are apparent:

- the dielectric material must not be susceptible to moisture absorption
- the process of photolithographic exposure and etching of the dielectric material must be simple while no a few residual gasses remain after the etch of the dielectric has been completed
- the profiles of trenches or openings that are etched in the dielectric material must be well defined and readily controllable
- be temperature independent

- provide good electrical isolation (low dielectric constant) between adjacent conducting materials that are embedded in the layer of dielectric, this up to very high frequencies
- must provide good protection against leakage currents between adjacent conducting materials
- must provide high resistance against electrical voltage breakdown between adjacent conducting materials
- must have good adhesion to underlying layers and provide good adhesion to overlying layers, and
- dielectric performance must not be temperature dependent.

It is clear that a simple and dependable method, that can be used for the identification and measurement of the performance characteristics of dielectric materials, is a valuable tool in a semiconductor manufacturing environment. The invention provides such a method.

US 5,386,507 (Teig et al.) shows a Computer graphics system for selectively modeling molecules and investigating the chemical and physical properties.

US 6,008,906 (Maris) shows a model that uses light measurement to predict dopant concentration, trap densities, etc.

US 5,687,090 (Chen et al.) shows a polymer simulation software that uses structural units to predict thermo-physical properties.

SUMMARY OF THE INVENTION

A principle objective of the invention is to characterize dielectric thin film properties by using chemical bonding measurements.

In accordance with the objectives of the invention a new computer based method is provided for the evaluation of dielectric film properties. These properties are for a given dielectric derived from measurements of the chemical bonding of that dielectric. Previously collected reference data are maintained in a reference data base from where data are extracted and used as input to mathematical modeling software that predicts thin film properties. The output of these prediction algorithms is used, together with chemical bonding measurements of the dielectric that is being investigated, as input to a program that computes the dielectric properties of the dielectric.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a set of graphic presentations of the effects of CVD chemical bonding on the dielectric constant k of various dielectric materials.

Fig. 2 shows a set of graphic presentations of the effects of CVD chemical bonding on the flat band voltage V_{fb} of various dielectric materials.

Fig. 3 shows the correlation between measured and calculated values for the dielectric constant k for carbon doped SiO_2.

Fig. 4 shows the correlation between measured and calculated values for the flat band voltage V_{fb} for carbon doped SiO_2.

Fig. 5 shows the effects of CVD chemical bonding on the dielectric constant k of carbon doped SiO_2 dielectric.

Fig. 6 shows the effects of CVD chemical bonding on the flat band voltage V_{fb} of carbon doped SiO_2 dielectric.

Fig. 7 shows a correlation between measured values and predicted values for the Refraction Index (RI) of carbon doped SiO_2 dielectric.

Fig. 8 shows a correlation between measured values and predicted values for the Stress (ST) factor of carbon doped SiO_2 dielectric.

Fig. 9 shows the chemical bonding normalized values of carbon doped SiO_2 dielectric.

Fig. 10 shows the weighing factors that are applied for carbon doped SiO_2 dielectric, as follows:

Fig. 10a shows the weighing factor applied for the Refraction Index, while

Fig. 10b shows the weighing factor applied for the Stress factor.

Figs. 11 through 14 show the correlation between chemical bonding and electrical properties of a dielectric, this for both the measured correlation and the predicted correlation. Fig. 11 addresses the dielectric constant k, Fig. 12 addresses the flat band voltage V_{fb}, Fig. 13 shows the weighing factor that is

applied to k while Fig. 14 shows the weighing factor that is applied to V_{fb}.

Fig. 15 shows TEOS characterization, RI measured versus predicted.

Fig. 16 shows TEOS characterization, Stress measured versus predicted.

Fig. 17 shows the normalized values for the TEOS dielectrics.

Fig. 18a a shows the RI weighing applied to the TEOS dielectrics.

Fig. 18b a shows the Stress weighing applied to the TEOS dielectrics.

Fig. 19 shows a block diagram of the computational method of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 shows a set of graphic presentations of the effects of CVD chemical bonding on the dielectric constant k of various dielectric materials. The horizontal or X axis of the graph that is shown in Fig. 1 is subdivided in various dielectric materials, where for each of these materials is shown the effect that variation of chemical bonding has on the dielectric constant.

The various dielectric materials are represented by the sections a, b through section j along the X axis of Fig. 1. For each of the sections that are shown along the X axis, that is for a particular dielectric that is represented by that section, the dielectric chemical bonds are measured using the Fourier Transform Infrared (FTIR) method.

The vertical or Y axis of the graph represents the dielectric constant k of the various dielectric materials. The chemical bonding intensity for each material is measured by FTIR.

X-axis section	dielectric material	wavenumber
a	Si-O	450
b	Si-O	820
c	Si-H	880

d	SiF	932
e	Si-O	1050
f	$Si-CH_3$	1243
g	Si-H	2250
h	CH	3000a
i	Si-NH	3400
j	OH	3680

From the graph that is shown in Fig. 1, a few conclusions can be drawn:

1) chemical bonding intensity varies between different materials

2) a steeper slope of the exposure (X axis) versus k (Y axis) indicates increased sensitivity of the chemical bond to the dielectric constant (k)

3) a higher slope of the curve (k versus chemical bonding intensity) indicates that a higher bonding intensity increases the k value in the dielectric material

4) for some dielectric materials the value of k increases (and with that the value of the bonding intensity of the material) with chemical bonding intensity while for other dielectric materials the inverse is true, and

5) the rate of increase or decrease of the various curves is not uniform but varies from material to material.

Fig. 2 shows a set of graphic presentations of the effects of CVD chemical bonding on the flat band voltage V_{fb} of various dielectric materials. The values and materials that are plotted along the X axis of Fig. 2 are identical to those of Fig. 1, the Y axis of Fig. 2 represents the flat band voltage V_{fb} of the dielectric. Observations can be made relative to the graphs that are shown in Fig. 2 that are similar to the previously made observations with respect to Fig. 1. It is of interest to note that, for most of the dielectric materials that are represented in Figs. 1 and 2, the slopes of the curves of Fig. 1 and Fig. 2 for a given material is the same. This means that a dielectric material that shows for instance an increase in the value of k with chemical bonding intensity ue of V_{fb}. This is however not universally true, a fact that will become apparent by comparing sections c, h and j of Fig. 1 with like-named sections in Fig. 2. Where, for instance, in section c of Fig. 1, the k value increases with increased chemical bonding, the V_{fb} value (Fig. 2) increases. The same is true for sections (dielectric materials) h and j.

Fig. 3 shows the correlation between measured and calculated values for the dielectric constant k of carbon doped SiO_2 dielectric material. The measured values of the dielectric constant k are plotted along the Y axis as rectangles while the

values for k that are calculated in accordance with the method of the invention are plotted along the Y axis with circles. The individual wafers that have been used for the subject evaluation are listed by sequence number along the X axis, in other words one particular point along the X axis is one wafer (in the sequence number in which the various wafers were analyzed), for that wafer the measured and predicted values of k have been plotted along the Y axis. It is apparent from the values that are indicated in Fig. 3 that the correlation between measured and calculated values is excellent.

Fig. 4 shows the correlation between measured and calculated values for the flat band voltage V_{fb} of carbon doped SiO_2 dielectric material. The measured values of the flat band voltage V_{fb} are indicated by rectangles in Fig. 4 while the values for the flat band voltage V_{fb} that are calculated in accordance with the method of the invention are indicated with circles. The individual wafers that have been used for the subject evaluation are listed by sequence number along the X axis, in other words one particular point along the X axis is one wafer (in the sequence number in which the various wafers were analyzed), for that wafer the measured and predicted values of k have been plotted along the Y axis. It is apparent from the values that are

indicated in Fig. 4 that the correlation between measured and calculated values is excellent.

Fig. 5 shows the effects of chemical bonding on the dielectric constant k of carbon doped SiO_2 dielectric material. Fig. 5 shows, similar to Fig. 1, a set of graphic presentations of the effects of CVD chemical bonding on the dielectric constant k of various carbon doped SiO_2 dielectric materials. The horizontal or X axis of the graph that is shown in Fig. 5 is subdivided in various carbon doped SiO_2 dielectric materials, where for each of these materials is shown the effect that modified chemical bonding has on the dielectric constant. The vertical or Y axis of the graph represents the dielectric constant k of the various carbon doped SiO_2 dielectric materials. The chemical bonding for each carbon doped SiO_2 material is measure by FTIR. The list of materials and wavenumbers is as follows:

X-axis section	dielectric material	wavenumber
a	SiC,SiO,CH	800
b	SiO	1030
c	$SiCH_3$	1268
d	SiH	2184
e	CH	3000

From the graph that is shown in Fig. 5 the conclusion that can be drawn is that different chemical bonding intensities affect the dielectric constant (k). As some of the chemical bonding intensities increase, the k value can increase. Some chemical bonding intensities however can decrease the value of k as the chemical bonding intensities increase.

Fig. 6 shows a set of graphic presentations of the effects of CVD chemical bonding on the flat band voltage V_{fb} of various carbon doped SiO_2 dielectric materials. The values and materials that are plotted along the X axis of Fig. 6 are identical to those of Fig. 5, the Y axis of Fig. 6 represents the flat band voltage V_{fb} of the dielectric. Observations can be made relative to the graphs that are shown in Fig. 6 that are similar to the previously made observations with respect to Fig. 5.

Fig. 7 shows a correlation between measured values and predicted values using the method of the invention for the Refraction Index (RI) of carbon doped SiO_2 dielectric. The measured values of RI are indicated by rectangles in Fig. 7 while the values for RI that are calculated in accordance with the method of the invention are indicated with circles. The individual wafers that have been used for the subject evaluation are listed by sequence number along the X axis, in other words

one particular point along the X axis is one wafer (in the sequence number in which the various wafers were analyzed), for that wafer the measured and predicted values of k have been plotted along the Y axis. It is apparent from the values that are indicated in Fig. 7 that the correlation between measured and calculated values of RI is excellent.

Fig. 8 shows a correlation between measured values and predicted values for the Stress factor of carbon doped SiO_2 dielectric. The measured values of Stress (ST) are plotted along the Y axis and are indicated by rectangles in Fig. 8 while the values for ST that are calculated in accordance with the method of the invention are plotted along the Y axis and are indicated with circles. The individual wafers that have been used for the subject evaluation are listed by sequence number along the X axis, in other words one particular point along the X axis is one wafer (in the sequence number in which the various wafers were analyzed), for that wafer the measured and predicted values of k have been plotted along the Y axis. It is apparent from the values that are indicated in Fig. 8 that the correlation between measured and calculated values of ST is excellent.

Fig. 9 shows the normalized values of carbon doped SiO_2 dielectric. The various normalization factors that are applied

under the method of the invention relate to the conditions that have been detailed in Figs. 5 and 6 above, that is normalization conditions highlighted with "a" are the normalization conditions that apply for SiC, SiO, Ch exposed with infrared of 800 MHz. The normalization conditions that are highlighted in Fig. 9 as "b", "c", "d" and "e" correspondingly relate to the conditions that are highlighted as such in Figs. 5 and 6.

Fig. 10 shows the weighing factors that are applied for carbon doped SiO_2 dielectric using the method of the invention, as follows:

Fig. 10a shows the weighing factor applied for the Refraction Index (RI), while

Fig. 10b shows the weighing factor applied for the Stress (ST) factor.

The regions that are highlighted with "a", "b", "c", "d" and "e" refer to the same conditions of dielectric material that have previously been highlighted under Figs. 5, 6 and 9.

Figs. 11 through 14 show the correlation between chemical bonding and electrical properties of a dielectric, this for both the measured correlation and the predicted correlation. Fig. 11 addresses the dielectric constant k, Fig. 12 addresses the flat

band voltage V_{fb}, Fig. 13 shows the weighing factor that is applied to k while Fig. 14 shows the weighing factor that is applied to V_{fb}. The individual wafers that have been used for the subject evaluation are listed by sequence number along the X axis, in other words one particular point along the X axis is one wafer (in the sequence number in which the various wafers were analyzed), for that wafer the measured and predicted values of k have been plotted along the Y axis. It can again be concluded that the correlation that is shown in Fig. 11 and 12 is very good correlation between the measured and the predicted values for both k and V_{fb}. The weighing factors that are shown have been applied to a selected list of dielectric materials that are selected from the dielectric materials that have first been shown under Fig. 1, as follows:

highlighted	dielectric material	wavenumber
a	Si-O	450
b	Si-O	820
c	Si-O	1050
d	$Si-CH_3$	1243
e	CH	3000

Figs. 15 and 16 address a practical verification of the method of the invention by evaluating the correlation for RI and

Stress of a layer of TEOS, the correlation is between measured values for these parameters and predicted values for these parameters in accordance with the method of the invention. Fig. 15 shows TEOS characterization, RI measured versus predicted. The measured values of RI are indicated by rectangles in Fig. 15 while the values for RI that are calculated in accordance with the method of the invention are indicated with circles. Fig. 16 shows TEOS characterization, Stress measured versus predicted. It is apparent from the values that are indicated in Figs. 15 and 16 that the correlation between measured and calculated values of RI for TEOS is excellent. The X axis serves the same function as previously has been highlighted, that is to indicated the various wafers that have been analyzed for the stated purpose.

Fig. 17 shows the normalized values for the TEOS dielectrics. The various normalization factors and weighing factors that are applied in Fig. 17 under the method of the invention relate to the conditions that have been detailed in Fig. 13 above, that is normalization conditions highlighted with "a" are the normalization conditions that apply for Si-O exposed with infrared of 450 wavenumber. The normalization conditions that are highlighted in Fig. 17 as "b", "c", "d" and "e" correspondingly relate to the conditions that are highlighted as such in Figs. 13.

Fig. 18 shows the weighing factors that are applied for TEOS dielectrics using the method of the invention, as follows:

Fig. 18a shows the weighing factor applied for the Refraction Index, while

Fig. 18b shows the weighing factor applied for the Stress factor.

The weighing factors that are highlighted in Fig. 18a and 18b as "a", "b", "c", "d" and "e" relate to the conditions of materials that are highlighted as such under Fig. 13.

Fig. 19 shows a block diagram of the computational method of the invention.

It should from the previous discussions be clear that there is a close and definite relationship between chemical bonding properties of a dielectric and their electrical properties, this is for instance clear from the correlation that has been established between these two entities as shown in Figs. 11 and 12. The effects that chemical bonding has on dielectric performance characteristics such as the dielectric constant k and the flat band voltage V_{fb} of the dielectric has also been established, see for instance Figs. 1 and 2. Once the chemical bonding of a dielectric film is known, other characteristics of

this dielectric film such as the dielectric constant k and V_{fb} can be derived from which dielectric characterization parameters such as the Refraction Index and the Stress Coefficient can be calculated. It is this interdependence between the various parameters that characterize a layer of dielectric that is used for the computational model of the invention. This computational model is highlighted in Fig. 19. The even numbered entities that are highlighted in Fig. 19 are software packages or programs that are computer based, the odd numbered entities are interconnects between the various functions of the computational model which henceforth will be referred to as a Dielectric Analysis Program (DAP).

The central function of the DAP system is function 10, the Dielectric Property Computation (DPC) program. Input to this program are the Chemical Bonding Measurements 12 that are provided to the DPC function 10 by means of interface 11. Interface 11 can be any currently available method of, among other functions, accessing a program and providing data to or extracting data from that program. Further input to the DPC function 10 is the output of the Behavioral Prediction Algorithms (BPA) function 16, this input is provided to DPC function 10 by means of the interconnect 17. The Established Data Base 14 is the central repository of data that relates to dielectric materials

and there depositions, such as previously have been highlighted. This data base 14 is updated with any data that has been obtained during the execution of the DAP functions, key among these data are CBM data 12 (supplied to the EDB via link 13) that have been obtained for a deposited layer of dielectric while dielectric properties 18 that have been obtained by the DAP system for a given layer of dielectric are stored (supplied to the EDB via link 21) and maintained in data base 14 for future reference. This data may also be accessed via link 15 as input to the BPA function 16. Output link 19 provides the predicted Dielectric Properties 18 to a ultimate user of the DAP functions.

Although the invention has been described and illustrated with reference to specific illustrative embodiments thereof, it is not intended that the invention be limited to those illustrative embodiments. Those skilled in the art will recognize that variations and modifications can be made without departing from the spirit of the invention. It is therefore intended to include within the invention all such variations and modifications which fall within the scope of the appended claims and equivalents thereof.